**module parity\_det (x, clk, z);**

**input x, clk;**

**output z; reg z;**

**reg even\_odd;**

**parameter EVEN = 0, ODD = 1;**

**always @(posedge clk)**

**case (even\_odd)**

**EVEN: begin**

**z <= x? 1:0;**

**even\_odd <= x? ODD:EVEN;**

**end**

**ODD: begin**

**z <= x? 0:1;**

**even\_odd <= x? EVEN:ODD;**

**end**

**default: even\_odd <= EVEN;**

**endcase**

**endmodule**

**module tst\_parity\_det;**

**reg x, clk;**

**wire z;**

**parity\_det pd (x, clk, z);**

**initial begin**

**clk = 0;**

**forever begin**

**#10 clk = ~clk;**

**#3 clk = ~clk;**

**end**

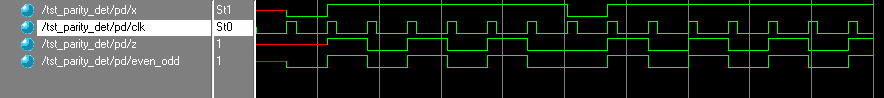
**end**

**initial**

**repeat (10) @(posedge clk)**

**x = $random;**

**endmodule**

****